DOUBLE WIDTH DATA BUS, SINGLE RATE TO SINGLE WIDTH DATA BUS, DOUBLE RATE CONVERTER CIRCUIT

Abstract

A converter circuit for converting a double width data bus (transmitting data at a single rate) to a single width data bus (transmitting data at a double rate). The circuit operates with a single clock, using the clock (positive clock) and its complement phase (negative clock) to process a set of even data and odd data. The circuit has a data mixer stage and an XOR stage. Even and odd data are mixed, using multiplexors and the positive and negative clocks, to generate mixed data. An XOR function is performed on the mixed data, using NAND gates. Using NAND gates to perform the XOR instead of a multiplexor ensures synchronous output timing, and ensures that the two stages are fully testable according to any scan-chain test method.